

Fig. 1

Replacement Sheet 2 of 6
Application: 10/065,340
Inventor: Stephen W. Melvin
Title: Hardware Enforced Virtual Sequentiality

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No Overlap Possible	Rd A		Packet #1 Processing		Wr A					
						Rd A		Packet #2 Processing		Wr A
Non-Optimal Overlap		Rd A	Packet #1 Processing	Wr A						
		•					Rd A	Packet #2 Processing	Wr A	į
Optimal Overlap		Rd A	Packet #1 Processing	Wr A						
·	[1.	Rd A	Packe Proces		Wr A		
Alternate Ordering Optimal			Rd	Pa	 cket #2	2 Wr	Rd A	Packet #1 Processing	Wr A	
Overlap			A		cket #2 cessin					

Fig. 2

Replacement Sheet 3 of 6 Application: 10/065,340 Inventor: Stephen W. Melvin

Title: Hardware Enforced Virtual Sequentiality

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300

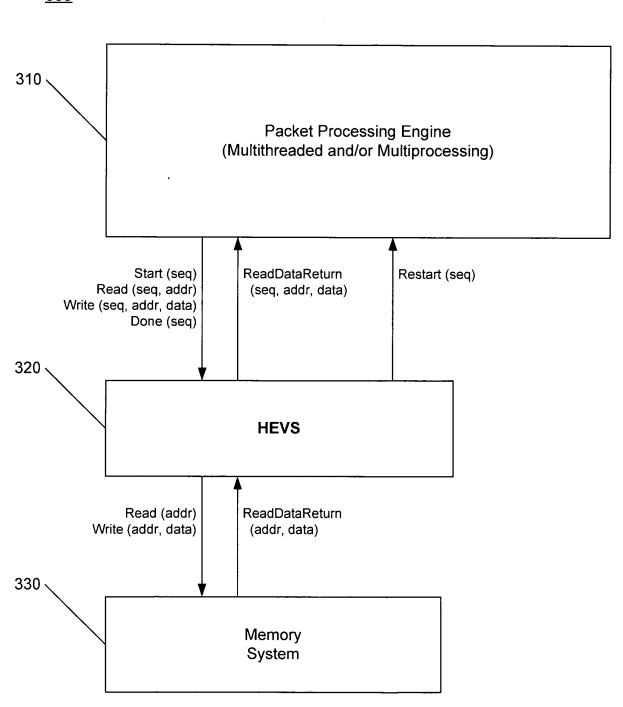


Fig. 3

Replacement Sheet 4 of 6 Application: 10/065,340 Inventor: Stephen W. Melvin

Title: Hardware Enforced Virtual Sequentiality

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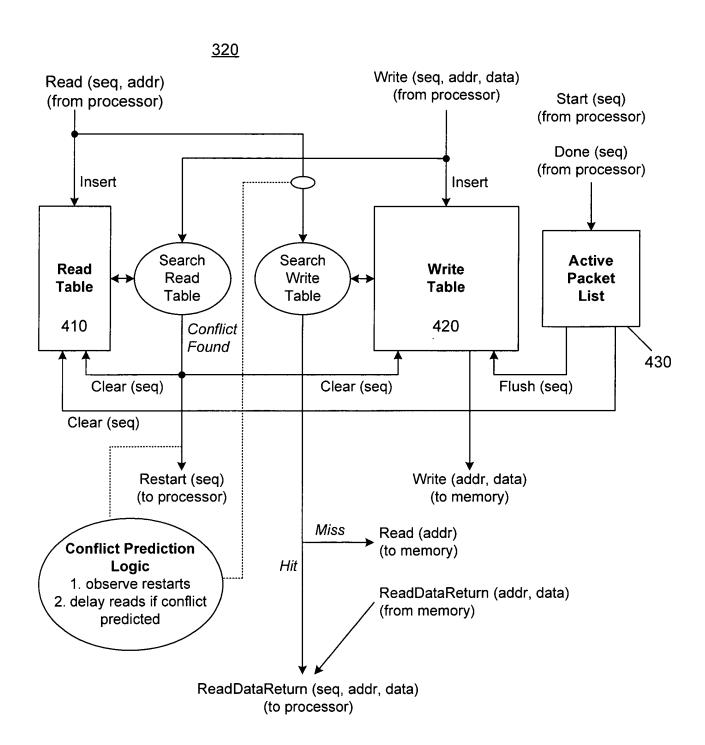


Fig. 4

Replacement Sheet 5 of 6 Application: 10/065,340 Inventor: Stephen W. Melvin

Title: Hardware Enforced Virtual Sequentiality

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Read Table Write Table

410		Seq.	Addr.		
F): -	1	A		
	1: [2	В		
9	::	3	В		
1	:: [2	Α		
	L				

	Seq.	Addr.	Data	Depend	420
	50.00				
:	2	В	Х	3	
ı:	1	A	Х	(null)	
-	•			(11411)	

400

Time Sequence:

1. Packet #1 reads location A

Entry p: created in Read Table

Write Table is searched, no matches found so memory read is performed

2. Packet #2 reads location B

Entry q: created in Read Table

Write Table is searched, no matches found so memory read is performed

3. Packet #2 writes location B

Entry r: created in Write Table

Read Table is searched, no conflicts found

4. Packet #3 reads location B

Entry s: created in Read Table

Write Table is searched, entry r: found, data X forwarded and dependency list updated

5. Packet #2 reads location A

Entry **t**: created in Read Table

Write Table is searched, no matches found so memory read is performed

6. Packet #1 writes location A

Entry u: created in Write Table

Read Table is searched for newer sequence read, entry **t**: is found Conflict is signaled to processor, Packet #2 is restarted Entry **q**: and all other sequence 2 entries are deleted Deletion of entry **r**: triggers Packet #3 restart signaled

Replacement Sheet 6 of 6 Application: 10/065,340 Inventor: Stephen W. Melvin

Title: Hardware Enforced Virtual Sequentiality

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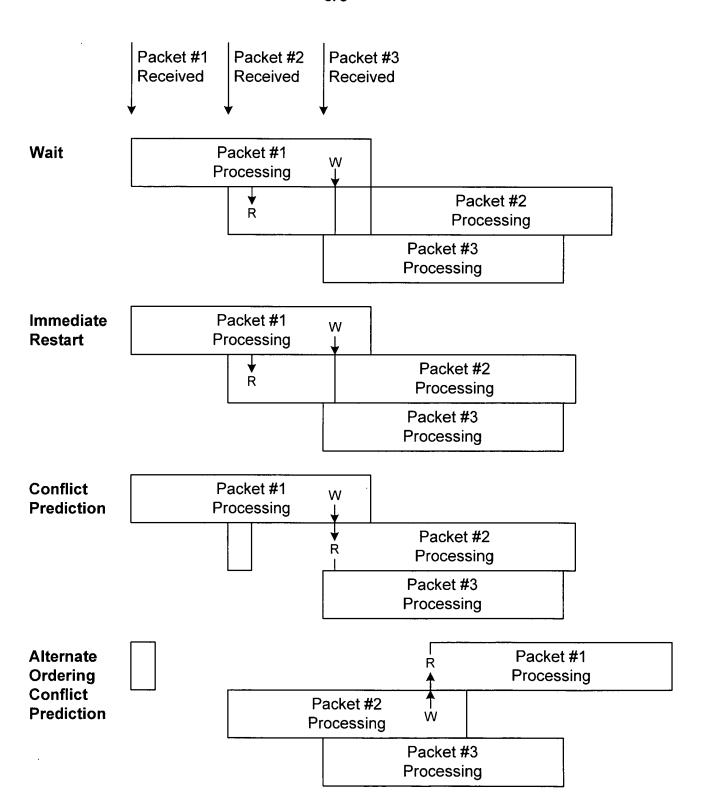


Fig. 6